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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,299	11/08/2001	Takashi Hiroi	501.40830X00	5170

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EXAMINER	
STREGE, JOHN B	
ART UNIT	**PAPER NUMBER**
2625	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,299	HIROI ET AL.	
	Examiner	Art Unit	
	John B. Strege	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28,29 and 31-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28,29 and 31-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/12/05 has been entered.

Terminal Disclaimer

The terminal disclaimer filed on 9/16/05 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on case 09/986,577 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Response to Amendment

The amendment received on 9/16/05 has been entered in full.

DETAILED ACTION

Claim Rejections - 35 USC § 102/103

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 28-29, and 38-40 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Gallarda et al. USPN 6,539,106 (hereinafter "Gallarda").

Regarding claim 28, Gallarda discloses a pattern inspection method comprising the steps of: attaining a digital image of an object substrate through microscopic observation thereof (col. 3 lines 23-29, and col. 16 lines 27-34 disclose that the test image can be from a scanning-electron-microscope); detecting defects of a pattern formed on said object substrate by comparing said digital image with a reference image stored in a memory while masking a preregistered region or a pattern matching with a pre-registered pattern (col. 3 lines 19-55 disclose preparing a reference image and a test image, extracting features from the reference image and extracting features from the test image, and comparing features of the reference image and of the test image to identify defects, wherein the extracting features from an image can comprise matching a feature template in the image and identifying features in the image that match the

feature-template [the template is a preregistered region (col. 6 lines 6-25) used to exclude data thus can be read as a mask]); and displaying intermediate images and results such as a map of defects and statistics about defect location, size, type, etc., are optionally displayed for monitoring by a human operator on a display screen 350 (figure 3 numeral 345 discloses a display for outputting a defect map, defect location, size, type, etc., col. 6 lines 26-35).

Gallarda discloses using a guided user interface (GUI, figure 3, col. 6 lines 6-9) to carry out the inspection and further that intermediate images and results such as a map of defects and statistics about defect location, size, type, etc. are shown on the display (col. 6 lines 26-35). The map of the defects comes from the actual images of the patterned substrates (as seen in figure 3), thus as a map of the defects is shown this map constitutes actual image data of each of the detected defects. Thus each of the defects on the map can be read as an actual image of a defect among the defects detected.

Gallarda does not explicitly disclose that the preregistered region or pattern is inputted and displayed on a display screen, however Gallarda does disclose the template region (the template is a preregistered region) which is a region found within the semiconductor wafer. As the map of the defects is displayed then the feature regions of the template must also be displayed on the map, thus reading on the limitation of displaying the pre-registered region on the display screen.

Regarding claim 29, Gallarda discloses that the reference image and test image can be obtained using a scanning-electron-microscope (col. 16 line10-34) and a feature

template can be used to aid in the feature extraction for a particular type of image can be used to extract the features (col. 17 lines 45-59), thus it is inherent that if the feature template is to be used with a microscopic reference and test images then it must be inputted using a microscopic image.

Regarding claim 38, Gallarda discloses a pattern inspection method comprising the steps of: attaining a digital image of an object substrate through microscopic observation thereof (col. 3 lines 23-29, and col. 16 lines 27-34 disclose that the test image can be from a scanning-electron-microscope); detecting candidate defects by processing the attained digital image (the image is processed by matching features of the test image to the reference image); extracting defects form the detected candidate defects by excluding candidate defects located in a predefined region on the object substrate or having a pattern that matches with a pre-registered pattern (col. 3 lines 53-55); displaying an image of a defect among the extracted defects on a display screen together with positional distribution data on the object substrate and feature quantity data thereof (figure 3 numeral 345 discloses a displaying a defect map, defect location, size, type etc.), classifying the defect which is displayed on said display screen (figure 3 numeral 345 discloses the type of defect [classification] is displayed); outputting class data of the classified defect together with feature quantity data thereof (figure 3 numeral 340 discloses outputting the defect size and type to memory).

Regarding claim 39, class data (type) of the classified defects is displayed (figure 3 numeral 340).

Regarding claim 40, the defect map is an image and is used as a judgement of the defects on the patterned substrate (col. 5 line 47- col. 6 line 5).

4. Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 in view of Matsui et al. USPN 5,850,467 (hereinafter "Matsui").

Gallarda discloses a pattern inspection method comprising the steps of: attaining a digital image of an object substrate through microscopic observation thereof (col. 3 lines 23-29, and col. 16 lines 27-34 disclose that the test image can be from a scanning-electron-microscope); detecting defects of a pattern formed on said object substrate by comparing said digital image with a reference image stored in a memory; and displaying data on the defects detected on a display screen (figure 3 numeral 345); wherein at the step of displaying a positional distribution of the defects on said object substrate is displayed on the display screen while excluding defects having a feature that matches with a pre-registered feature or distinguishing from defects which do not have a feature that matches with the pre-registered feature (col. 3 lines 19-55 disclose preparing a reference image and a test image, extracting features from the reference image and extracting features from the test image, and comparing features of the reference image and of the test image to identify defects, wherein the extracting features from an image can comprise matching a feature template in the image and identifying features in the image that match the feature-template [thus excluding nuisance defects having a feature that matches with a pre-registered feature], figure 3 numeral 345 discloses a

display for outputting a defect map, defect location, size, type, etc.). This leads to a reduced rate of nuisance defects and false defects, and increased sensitivity to killer defects (col. 5 lines 45-50).

Gallarda discloses using a guided user interface (GUI, figure 3, col. 6 lines 6-9) to carry out the inspection and further that intermediate images and results such as a map of defects and statistics about defect location, size, type, etc. are shown on the display (col. 6 lines 26-35). The map of the defects comes from the actual images of the patterned substrates (as seen in figure 3), thus as a map of the defects is shown this map constitutes actual image data of each of the detected defects. Thus each of the defects on the map can be read as an actual image of a defect among the defects detected.

Gallarda does not explicitly disclose that the preregistered region or pattern is inputted and displayed on a display screen, however Gallarda does disclose the template region (the template is a preregistered region) which is a region found within the semiconductor wafer. As the map of the defects is displayed then the feature regions of the template must also be displayed on the map, thus reading on the limitation of displaying the pre-registered region on the display screen.

Gallarda does not explicitly disclose displaying an enlarged image of a defect among the defects detected. Matsui discloses that it is difficult to detect an extremely small defect when inspecting a reticle (col. 2 lines 41-50). To remedy this problem Matsui discloses enlarging the defect such as seen in figures 4a and 4c (col. 5 lines 11-17). This enables for very small defects to be detected.

Gallarda and Matsui are analogous art because they are from the same field of endeavor of semiconductor inspection using image processing.

At the time of the invention it would have been obvious to one of ordinary skill in the art to modify Gallarda to display an enlarged image of a defect. The motivation for doing so is that it would make it easier for the operator to detect the small defects. Thus it would have been obvious to one of ordinary skill in the art to combine Gallarda and Matsui to obtain the invention as specified in claim 31.

Regarding claim 32, Gallarda discloses that the reference image and test image can be obtained using a scanning-electron-microscope (col. 16 line10-34) and a feature template can be used to aid in the feature extraction for a particular type of image can be used to extract the features (col. 17 lines 45-59), thus it is inherent that if the feature template is to be used with a microscopic reference and test images then it must be set up using a microscopic image.

Regarding claim 33, Gallarda discloses a defect map thus displaying the defect on the display (figure 3 numeral 345).

Claim 34 is similar to claim 31 with the extra limitation that data regarding defects located in a preregistered area is output so as to be distinguishable from data regarding an other detected defect. Gallarda discloses displaying a map of defects and their positional data (figure 3 numeral 345, and col. 6 lines 32-35). As the display is a map it is possible to distinguish one defect from another defect based on its position on the map.

Regarding claim 35, Gallarda discloses that the reference image and test image can be obtained using a scanning-electron-microscope (col. 16 line10-34) and a feature template can be used to aid in the feature extraction for a particular type of image can be used to extract the features (col. 17 lines 45-59), thus it is inherent that if the feature template is to be used with a microscopic reference and test images then it must be set up using a microscopic image.

Regarding claim 36, positional data of the defects is displayed on a display screen with an image of the other detected defects (figure 3 numeral 345).

Regarding claim 37, feature data includes defect position (figure 3 numeral 345).

5. Claims 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 in view of Ikenega USPN 4,989,156.

Gallarda does not explicitly disclose that the feature quantity is displayed on a CAD terminal, however does discuss that the feature data is outputted for an operator (col. 6 lines 30-35) and furthermore that the reference data can come from CAD data (col. 16 lines 10-26).

It is well known to display design information to CAD so that it may be modified by an operator. Ikenaga discloses outputting CAD data so that an operator can visually check a wafer pattern and then modify the data (col. 4 lines 24-42).

Gallarda and Ikenaga are analogous art because they are both from the same field of endeavor of semiconductor design.

At the time of the invention it would have been obvious to display the defect map on a CAD terminal to allow the operator to make design changes. Thus it would have been obvious to one of ordinary skill in the art to combine Gallarda and Ikenaga to obtain the invention of claims 41-42.

Response to Arguments

Applicant's arguments filed 9/13/05 have been fully considered but they are not persuasive. Specifically the Applicants argue that Gallarda does not disclose an actual image of the defect. As the defect map is derived from an actual test image of the patterned substrate (see discussion above), it constitutes an actual image.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Strege whose telephone number is (571) 272-7457. The examiner can normally be reached on Monday-Friday between the hours of 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JS

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